Sense and Drive the World

SYN113/SYN115 Datasheet

(300-450MHz ASK Transmitter)

Version 1.0

Contents

1. General Description

The SYN113/SYN115 is a high performance, easy to use, single chip ASK Transmitter IC for remote wireless applications in the 300 to 450MHz frequency band. This transmitter IC is a true "data-in, antenna-out" monolithic device. SYN113/SYN115 has three strong attributes: power delivery, operating voltage and operating temperature. In terms of power, the SYN113/SYN115 is capable of delivering +10 dBm into a 50Ω load. This power level enables a small form factor transmitter (lossy antenna) such as a key fob transmitter to operate near the maximum limit of transmission regulations. In terms of operating voltage, the SYN113/SYN115 operates from 1.8V to 3.6V. Many transmitter ICs in the same frequency band stop operating below 2.0V. The SYN113/SYN115 will work with most batteries to the end of their useful limits. In terms of operating temperature, the SYN113/SYN115 operates from -40°C to +85°C.

The SYN113/SYN115 is easy to use. It requires a reference frequency (RF carrier frequency divided by 32 times) generated from a crystal with a few additional external parts to create a complete versatile transmitter.

The SYN113/SYN115 operates with ASK/OOK (Amplitude Shift Keying/On-Off Keyed) UHF receiver types from wide-band super-regenerative radios to narrow-band, high performance super-heterodyne receivers. The SYN113/SYN115's maximum ASK data rate is 10kbps (Manchester Encoding).

The SYN113/SYN115 transmitter solution is ideal for industrial and consumer applications where simplicity and form factor are important.

For enhanced power saving, SYN115 includes power managing function（SYN113 do not have this function）. The power managing function Enables transmitter activated as long as high transient data input trigger signals are received. The transmitter will also be automatically switched off if there are no data input transients for a time exceeding approximately 75ms.

2. Features

- Complete UHF transmitter
- Frequency range 300MHz to 450MHz
- Data rates up to 10kbps ASK
- Output Power to 10dBm
- Low external part count
- Low voltage operation (down to 1.8V)
- Operate with crystals or ceramic resonators
- Power down modes and wake-up functions to reduce power consumption（SYN115 only）

3. Applications

- Fan Controllers

- Remote Power Switches
- Multi-Media Remote Control
- Remote Sensor Data Links
- Infrared Transmitter Replacement

4. Typical Application

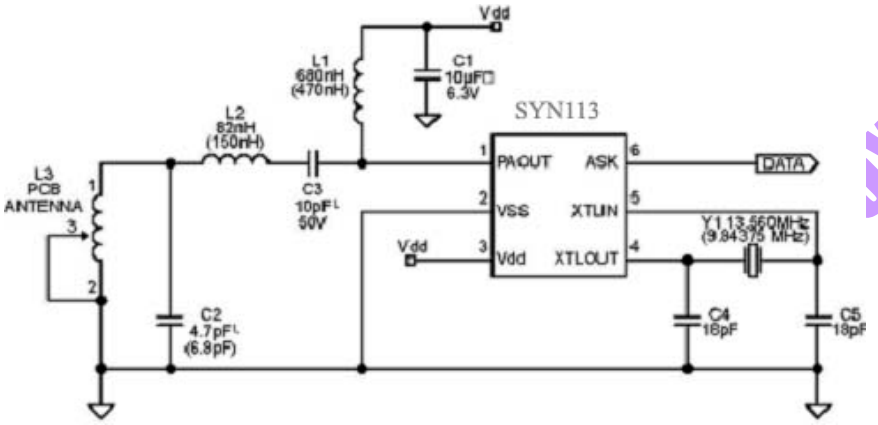
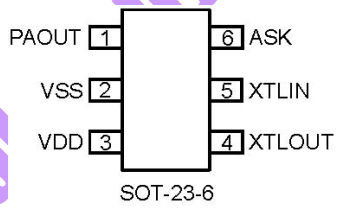


Figure 1. SYN113/SYN115 ASK Key Fob Design for 315 MHz and 433.92 MHz
(Note: Values indicated in parentheses are for 315MHz)

5. Pin Configuration



6. Pin Description

Pin Number SOT23-6	Pin Name	Pin Function
1	PA_OUT	Bandwidth Selection Bit 0 (Digital Input): Used in conjunction with SEL1 to set the desired demodulator filter bandwidth. See Table 1. Internally pulled-up to VDDRF
2	VSS	Ground
3	VDD	Voltage Drain Drain (Input): Positive Power Supply
4	XTLOUT	Crystal Out (Output): Reference oscillator output connection.
5	XTLIN	Crystal In (Input): Reference oscillator input connection.
6	ASK	ASK DATA Input

7. Absolute Maximum Ratings (1)

Supply Voltage (V_{DD})	+5V
Input/Output Voltage ($V_{I/O}$)	V_{SS}–0.3 to V_{DD}+0.3
Voltage on PA_OUT(V_{PA_OUT})	+7.2V
Storage Temperature Range (T_S)	–65°C to +150°C
Lead Temperature (soldering, 10 sec.)	+300°C
ESD Rating	2KV (3)

8. Operating Ratings (2)

RF Frequency Range	300MHz to 450MHz
Supply Voltage (VDD)	+1.8V to +3.6V
Ambient Temperature (T_A)	–40°C to +85°C

9. Electrical Characteristics (4)

Specifications apply for VDD = 3.0V, TA = 25°C, $Freq_{REFOSC}$ = 13.560MHz, EN = VDD. Bold values indicate –40°C to 85°C unless otherwise noted. 1kbps data rate 50% duty cycle. RL 50ohm load (matched)

Parameter	Condition	Min	Typ	Max	Units
Power Supply					
Mark Supply Current I_{ON}	@ 315MHz, POUT = +10dBm		12.3		mA
	@ 433.92MHz, POUT = +10dBm		12.5		mA
SPACE supply current, I_{OFF}	@ 315MHz		3		mA
	@ 433.92 MHz		3		mA
Standby Mode					
Standby supply current, I_{STB}	@ 315MHz			1	uA
	@ 433.92 MHz			1	uA
Standby delay time	ASK transition from HIGH to LOW	30	75	120	ms
	ASK transition from HIGH to LOW	30	75	120	ms
RF Output Section and Modulation Limits:					
Output power level, P_{OUT} ASK "mark"	@315MHz (4)		10		dBm
	@433.92MHz (4)		10		dBm

Harmonics output for 315 MHz	@ 630MHz [4] 2nd harm.		-39		dBc
	@945MHz [4] 3rd harm.		-53		dBc
Harmonics output for 433.92 MHz	@ 867.84MHz [4] 2nd harm.		-55		dBc
	@1301.76MHz [4] 3rd harm.		-55		dBc
Extinction ratio for ASK			70		dBc
ASK Modulation					
Data Rate				10	kbps
Occupied Bandwidth	@315MHz [6]		<700		kHz
	@433.92MHz [6]		<1000		kHz
VCO Section					
315 MHz Single Side Band Phase Noise	@ 100kHz from Carrier		-76		dBc/Hz
	@ 1000kHz from Carrier		-79		dBc/Hz
433.92 MHz Single Side Band Phase Noise	@ 100kHz from Carrier		-72		dBc/Hz
	@ 1000kHz from Carrier		-81		dBc/Hz
Reference Oscillator Section					
XTLIN, XTLOUT	Pin capacitance		2		pF
External Capacitance	See Schematic C17 & C18		18		pF
Oscillator Startup Time [5]	Crystal: HC49S		300		µs
Digital / Control Section					
Output Blanking	VDD transition from LOW to HIGH		500		µs
Digital Input ASK Pin	High (V_{IH})	$0.8\times V_{DD}$			
	Low (V_{IL})			$0.2\times V_{DD}$	V
Digital Input Leakage Current ASK Pin	High (V_{IH})		0.05		
	Low (V_{IL})		0.05		µA
Under Voltage Lock Out (UVLO)			1.6		

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.
4. Measured using Test Circuit in Figure
5. Dependent on crystal
6. RBW = 100kHz, OBW measured at -20dBc.

10. Test Circuit

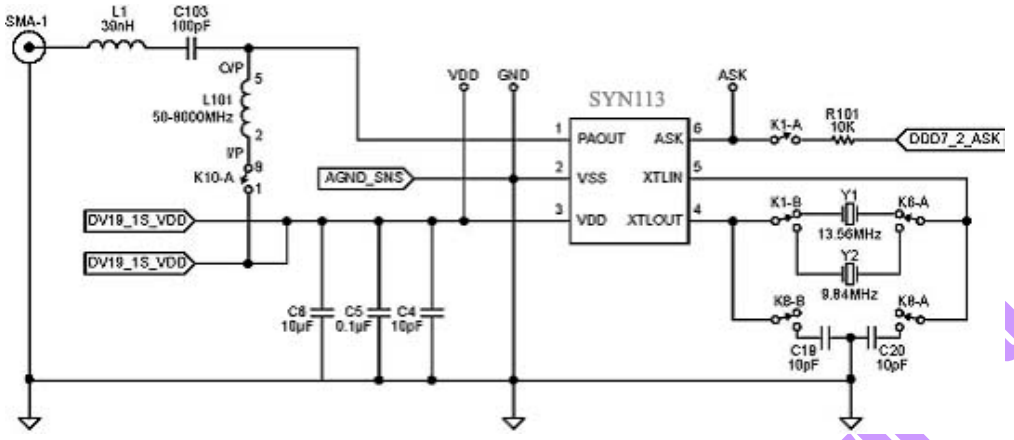
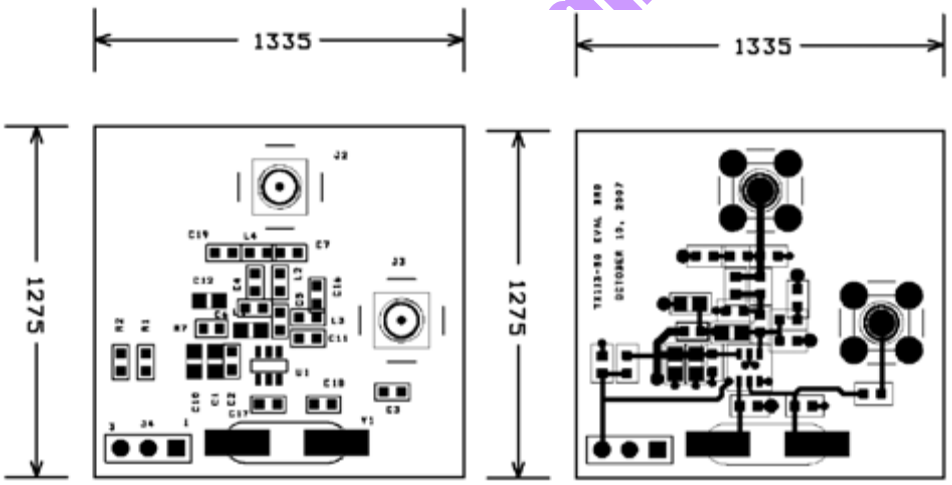


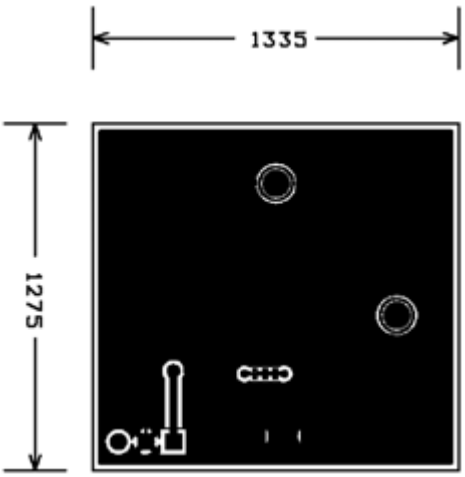
Figure 2. SYN113/SYN115 Test Circuit

11. SYN113/SYN115 PCB Layout Recommendations



Assembly Drawing
SYN113/SYN115 50Ohm Test Board

Top Layer
SYN113/SYN115 50Ohm Test Board



Bottom Layer

SYN113/SYN115 50Ohm Test Board

12. Functional Diagram

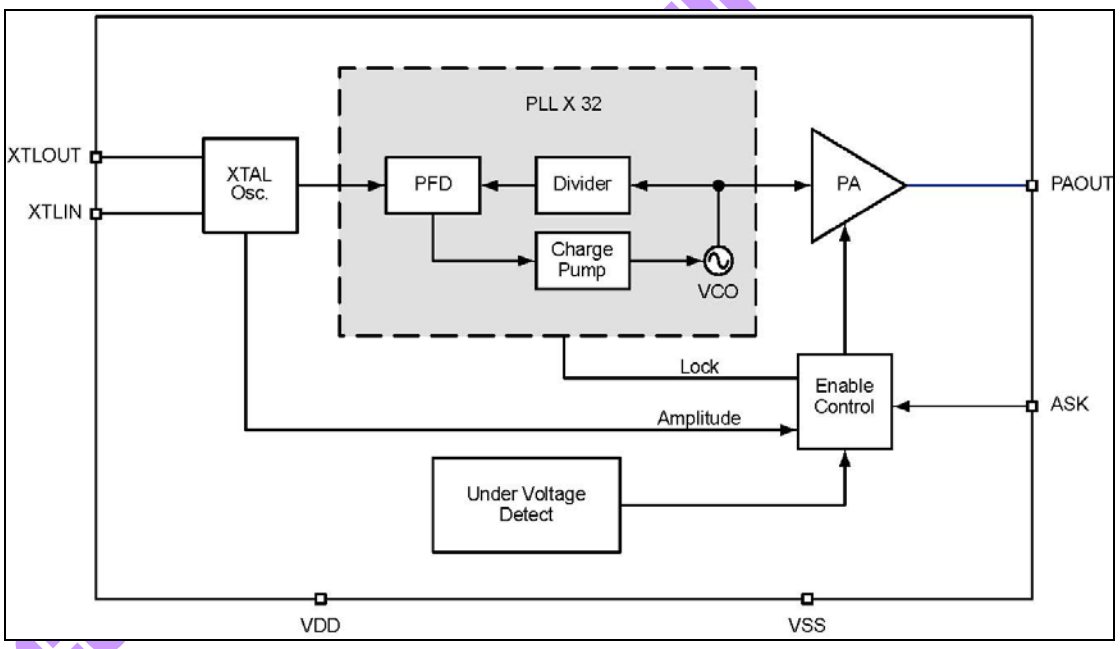


Figure 3. Functional Block Diagram SYN113/SYN115

13. Functional Description

Figure 3 is a functional block diagram of the SYN113/SYN115 transmitter. The SYN113/SYN115 is best described as a phase locked transmitter. The SYN113/SYN115 system is partitioned into five functional blocks:

- Crystal oscillator
- PLL×32
- Power amplifier
- Enable control
- Under voltage detection

13.1. Crystal Oscillator

The reference oscillator is crystal-based Pierce configuration, designed to accept crystals with frequency from 9.375MHz to 14.0625MHz.

13.1.1. Crystal Oscillator Parameters for ASK Operation

Figure 4 shows a reference oscillator circuit configuration for ASK operation. The reference oscillator is capable of driving crystals with ESR range from 20Ω to 300Ω.

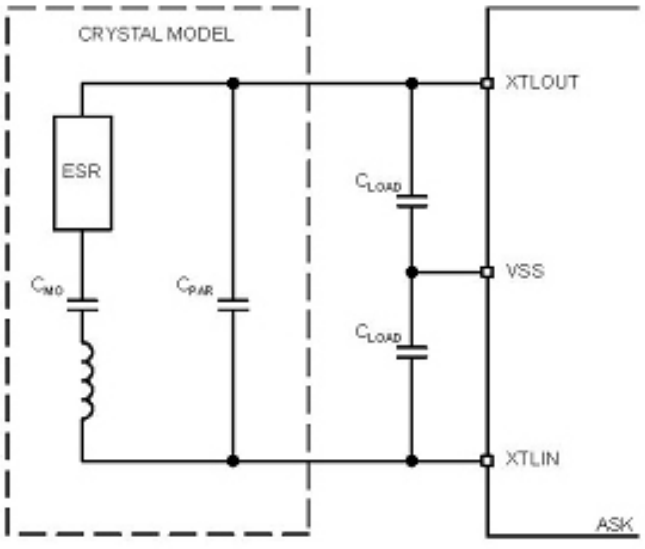


Figure 4. Reference Oscillator ASK Operation

- When the ESR of crystal is at 20Ω, the crystal parameter limits are:
  - ESR 20Ω

- C_{PAR} 2 to 10pF
- C_{MO} 10 to 40fF

- When the ESR of crystal is at 300Ω, the crystal parameter limits are:
  - ESR 300Ω
  - C_{PAR} 2 to 5pF
  - C_{MO} 10 to 40fF
  - C_{LOAD} 10 to 30pF

13.2. PLL ×32

The function of PLL×32 is to provide a stable carrier frequency for transmission. It is a "divide by 32" phase locked loop oscillator.

13.3. Power Amplifier

The power amplifier serves two purposes:

- To buffer the VCO from external elements
- To amplify the phase locked signal. The power amplifier can produce +10dBm at 3V (typical).

13.4. Enable Control

Enable control gates the ASK data. It only allows transmission when Lock, Amplitude and Under Voltage Detect conditions are valid.

13.5. Under Voltage Detect

"Under voltage detect" block senses operating voltage. If the operating voltage falls below 1.6V, "under voltage detect" block will send a signal to "enable control" block to disable the PA.

14. Application Information

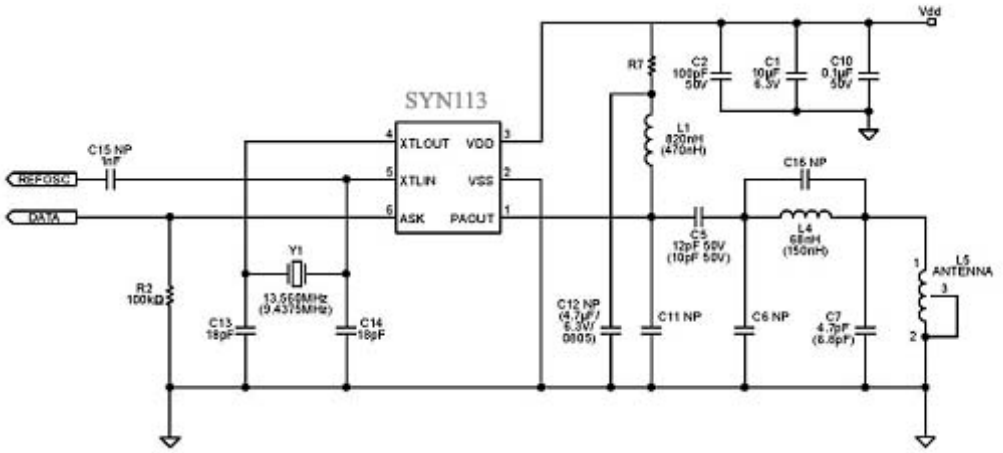


Figure 5. ASK 433.92MHz and (315MHz)

Notes:

1. Components labeled NP are not placed.
2. Values without parentheses are for 433.92 MHz and values in parentheses are for 315MHz.
3. Value of R7 is selected to vary the output power.

The SYN113/SYN115 is well suited to drive a 50-ohm source, monopole or a loop antenna. Figure 5 is an example of a loop antenna configuration. Figure 5 also shows both 315MHz and 433.92MHz ASK configurations for a loop antenna. Besides using a different crystal, Table 1 lists modified values needed for the listed frequencies.

Frequency (MHz)	L1 (nH)	C5 (pF)	L4 (nH)	C7 (pF)	Y1 (MHz)
315.0	470	10	150	6.8	9.84375
433.92	820	12	68	4.7	13.5600

Table 1

The reference design shown in Figure 5 has an antenna optimized for using the matching network as described in Table 1.

14.1. Power Amplitude Control Using External Resistor

R7 is used to adjust the RF amplitude output levels which may be needed to meet compliance regulation. As an example, the following tables list typical values of conducted RF output levels and corresponding R7 resistor values for the 50-ohm test board, as shown in Figure 2. R7 of the SYN113/SYN115 Demo board using the loop antenna can be adjusted for the appropriate radiated field allowed by FCC or ETSI compliance. Contact Synoxo for suggested R7 values to meet FCC and ETSI compliances.

R7, Ω	Output Power, dBm	IDD, mA
0	10	6.7
75	8.5	6.3
100	8.0	6.2
500	1.6	4.13
1000	-3.8	4.87

Output Power Versus External Resistor at 315MHz

R7, Ω	Output Power, dBm	IDD, mA
0	8.68	7.5
75	8.34	7.33
100	8.02	7.3
500	4.34	6.3
1000	0.42	5.5

Output Power Versus External Resistor at 433.92 MHz

14.2. Output Power ON-OFF Control

There are three ways to enable the PA output power. First, by supplying the ASK signal with VDD applied continuously, resulting in a Mark and Space RF output condition. Second method involves applying both VDD and ASK synchronously. The third way is using Power Manager Function. This function is for SYN115 only.

The second method allows for longer battery usage since the battery is disconnected during non-activation. Figure 6 shows the RF output time response since VDD and the ASK are applied to the SYN113/SYN115. The RF output response, as a function of VDD, is typically less than 1.25mSec. This measurement was done using the circuitry shown in Figure 2.

Note: The ASK signal should never be applied before VDD.

14.3. RF Output Response as a Function of VDD and ASK

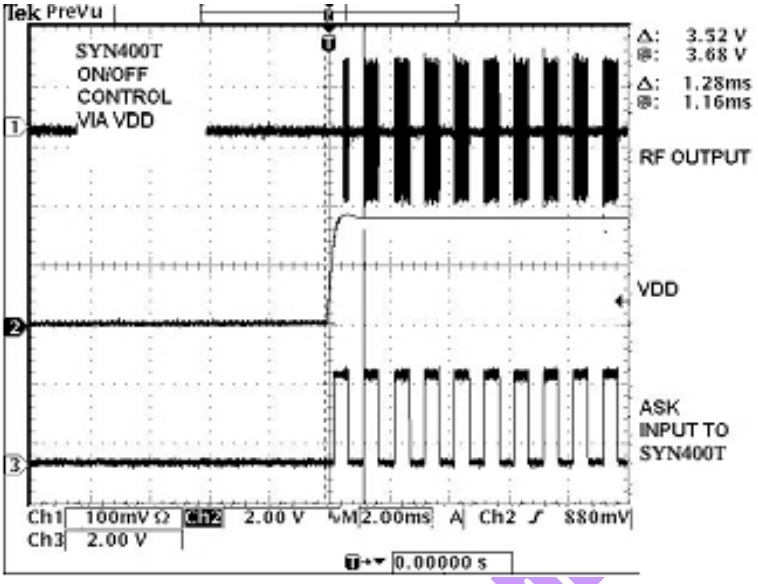


Figure 6. RF Output Response (VDD and ASK)

14.4. Output Matching Network

Part of the function of the output network is to attenuate the second and third harmonics. When matching to a transmit frequency, care must be taken both to optimize for maximum output power, and to attenuate unwanted harmonics.

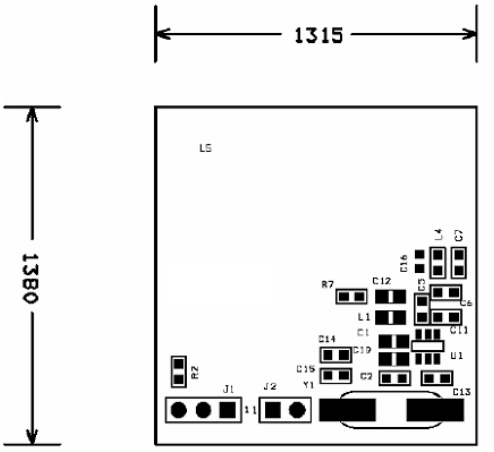
14.5. Layout Issues

PCB Layout is a primary concern for achieving optimum performance and consistent manufacturing results. Care must used with the orientation of components to ensure that they do not couple or decouple the RF signal. PCB trace length should be short to minimize parasitic inductance (1 inch ~ 20nH). For example, depending upon inductance values, a 0.5 inch trace can change the inductance by as much as 10%. To reduce parasitic inductance, the practice of using wide traces and a ground plane under the signal traces is recommended. Vias with low value inductance should be used for components requiring a connection-to-ground.

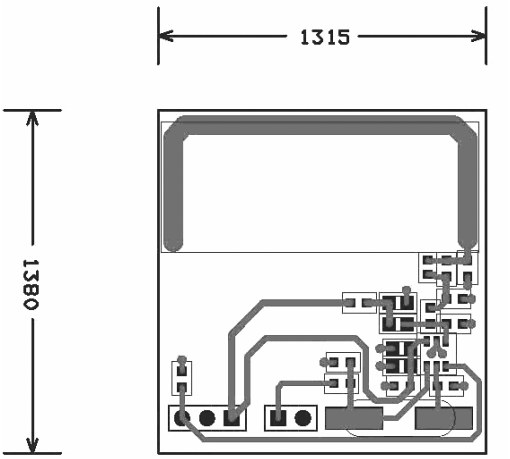
14.6. Antenna Layout

Directivity is affected by antenna trace layout. No ground plane should be under the antenna trace. For consistent performance, components should not be placed inside the loop of the antenna.

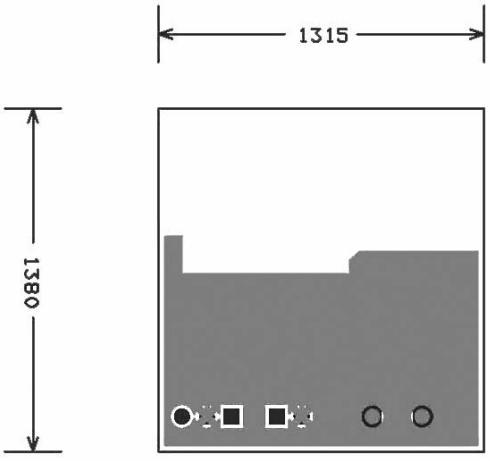
15. PCB Board



Assembly Drawing
SYN113/SYN115 Demo Board



Top Layer
SYN113/SYN115 Demo Board



Bottom Layer
SYN113/SYN115 Demo Board

Figer 7. Demo Board PCB

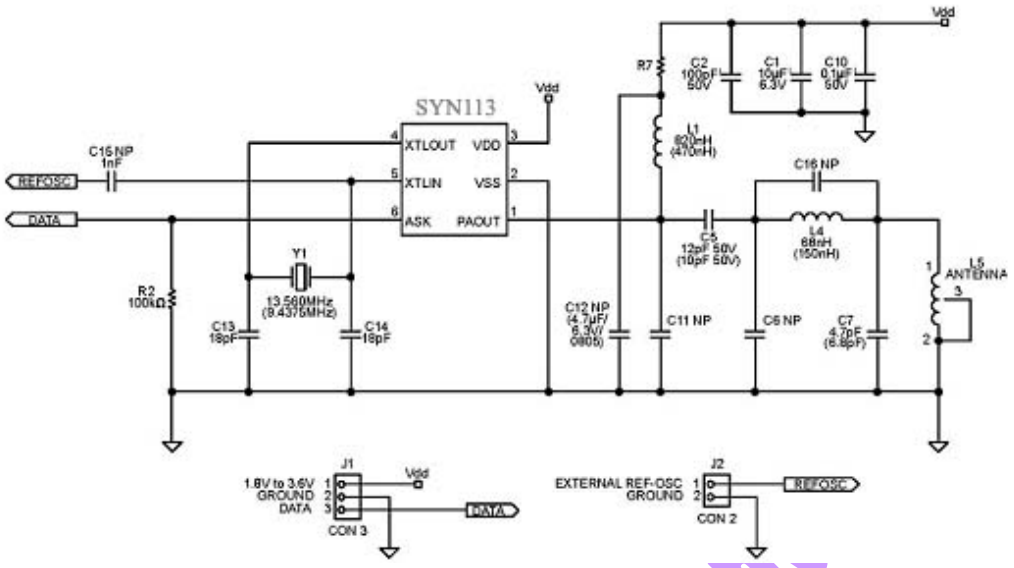


Figure 8. SYN113/SYN115 Demo Board Schematic

Notes:

1. Components labeled NP are not placed.
2. Values without parentheses are for 433.92 MHz and values in parentheses are for 315MHz.
3. Value of R7 is selected to vary the output power.

15.1 Functional Description of SYN113/SYN115 Evaluation Board.

Figure 7 shows the SYN113/SYN115 Demo Board PCB layout and assembly (Gerber format). Figure 8 is a detailed schematic of the SYN113/SYN115. Note that components labeled as NP (not placed) can be used to obtain different configurations. Table 2 describes each header pin connector used in the demo board.

Pin	Function Name	Functional Description
J1-1	VDD	1.8V to 3.6V input voltage
J1-2	VSS	Ground
J1-3	ASK	Modulating Data Input
J2-1	REF-OSC	External Reference Oscillator Input
J2-2	VSS	Ground

Table 2.

15.2. SYN113/SYN115-433.92 ASK Bill of Materials

Item	Quantity	Ref	Part	PCB Footprint	Mfg P/N	Manufacturer
1	1	C1	10μF	0805	GRM21BR60J106KE01L	muRata
2	1	C2	100pF	0603	GRM1885C1H101JA01D	muRata
3	1	C5	12pF	0603	GRM1885C1H100JA01D	muRata
4						
5	3	C6,C11,C16	(NP)			
6	1	C7	4.7pF	0603	GRM1885C1H4R7JA01D	muRata
7						
8	2	C13,C14	18pF	0603	GRM1885C1H180JA01D	muRata
9	1	J1	CON3		TSHR-114-S-02-A-GT	
10	1	L1	820nH	0805	0805CS-680XJB	Coilcraft
11	1	L4	68nH	0603	0603CS-082NXJB	Coilcraft
12	1	L5	ANTENNA		ANTENNA LOOP, Part of PCB	
13	1	R2	100kΩ	0603	CRCW0603100KFKEA	Vishay
14	1	R7	0Ω	0603	CRC06030000Z0EA	Vishay
13	1	U1	SYN113/SYN115Y		SYN113/SYN115	Synoxo
14	1	Y1	13.560MHZ XTAL		SA-13.5600-F-10-C-3-3	HIB

Table 3

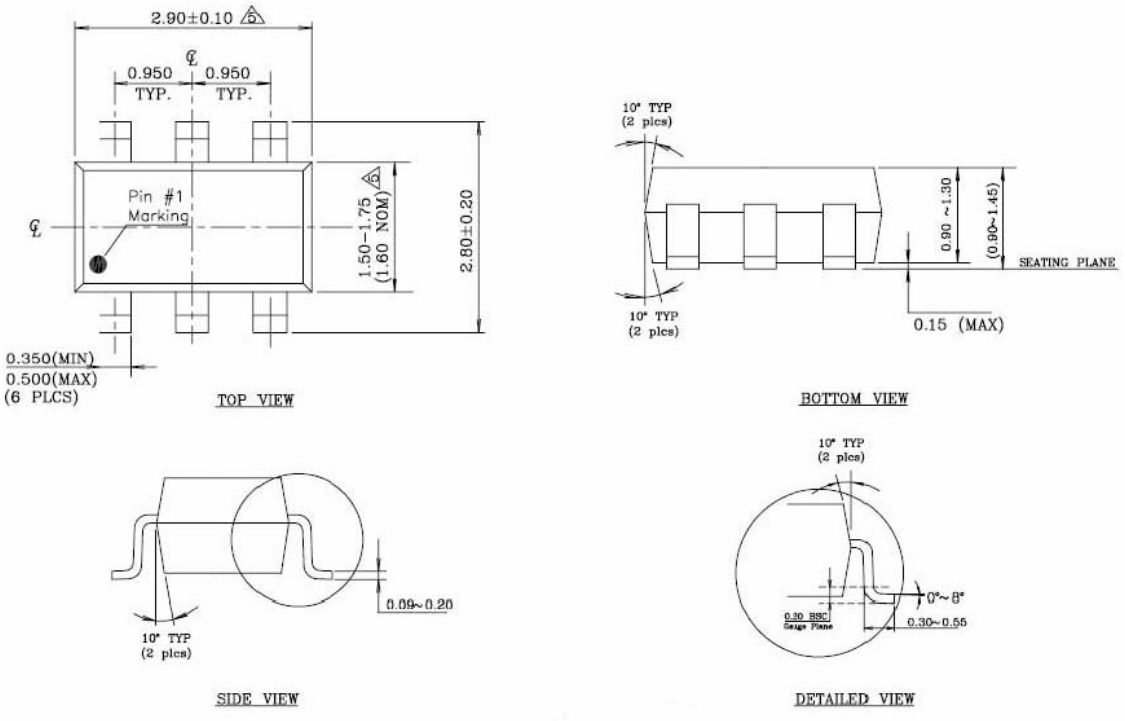
15.3. SYN113/SYN115-315MHz ASK Bill of Materials

Item	Quantity	Ref	Part	PCB Footprint	Mfg P/N	Manufacturer
1	1	C1	10μF	0805	GRM21BR60J106KE01L	muRata
2	1	C2	100pF	0603	GRM1885C1H101JA01D	muRata
3	1	C5	10pF	0603	GRM1885C1H1000JA01D	muRata

4						
5	3	C6,C11,C16	(np)			
6	1	C7	6.8pF	0603	GRM1885C1H6R8JA 01D	muRata
7	1	C10	0.1μF	0603	GRM188F51H104ZA 01D	muRata
8	2	C13,C14	18pF	0603	GRM1885C1H180JA 01D	muRata
9	1	J1,J2	CON3		TSHR-114-S-02-A-G T	
10	1	L1	470nH	0805	0805CS-470XJB	Coilcraft
11	1	L4	150nH	0603	0603CS-R15XJB	Coilcraft
12	1	L5	ANTENNA		ANTENNA LOOP, Part of PCB	
13	1	R2	100kΩ	0603	CRCW0603100KFK EA	Vishay
14	1	R7	0Ω	0603	CRC06030000Z0EA	Vishay
13	1	U1	SYN113/SY N115YMM 6		SYN113/SYN115	Synoxo
14	1	Y1	9.84375MH Z XTAL		SA-9.84375-F-10-C-3 -3	HIB

Table 4

16. Package Information



SOT23-6 Package

Notes:

1. Dimensions and tolerances are in accordance with ANSI Y14.5M, 1982.
2. Package surface to be mirror finish.
3. Die is facing up for mold. Die is facing down for trim/form, that is, reverse trim/form.
4. The footlength measuring is based on the gauge plane method.

Dimensions are exclusive of mold flash and gate burr.